TÜBİTAK

PROJE SONUÇ RAPORU

Silicon Carbide Based Three Phase Inverter With Higher; Efficiency, Power Capability and Power Density For Renewable Energy Applications

Program Kodu: 1002

Proje No: 119E149

Proje Yürütücüsü:
Asts. Prof. Bilal EID

Bursiyer(ler):
Hasan GÜDEN
Ahmet EREN

TEMMUZ 2020
GAZİANTEP

PREFACE

During the last 20 years Si-based IGBTs (Insulated Gate Bipolar Transistors) were widely used in power electronic devices. However, due to their physical and electrical limits Si based power modules couldn't gain more popularity as expected. Thus, many researches have been focused on improving the performance of this device. As a result of the previous researchers studies, Silicon carbide (SiC) and gallium nitride (GaN) based semiconductor devices with wide band gap started to stand out due to their high performance and higher power density.

There are three main physical characteristics of SiC semiconductor which makes it superior to ordinary Si devices, McBryde et al. (2010): 1) Lower leakage currents. Electron-hole pairs generates much slower in SiC than in Si. This will reduce the leakage current losses when the switch is off compared to Si at a given temperature. 2) Increased critical breakdown strength. This implies that the device can withstand a higher voltage in the same package, or the package insulation can be reduced at the same voltage rating. Devices like Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and Junction Field Effect Transistor (JFET) can thereby be created at blocking voltages approximately an order of magnitude higher than what is possible with Si, Elasser et al. (2002). 3) A higher thermal conductivity allows for more efficient transportation of heat from the device. Additionally, the on-state resistance through the switch is lower, causing decreased conducting losses. 4) Moreover, in conventional bipolar Si switches, e.g. insulated-gate bipolar transistor (IGBT), the switching frequency is limited by the time required for the plasma in the drift region to establish and be removed. For unipolar SiC devices this limit does not apply, allowing significantly higher switching frequencies, Anthony et al. (2014).

Based on the above mentioned reasons the aims of this project is to design and implementation of SiC based inverter. Three phase two-level high efficiency and power density inverter was developed to be suitable for renewable energy applications. As a design criterion grid frequency and input and output voltage range was chosen according to Turkey grid operation.

In this project, a SiC Based three phase inverter is developed. The developed inverter is light weighted with high efficiency and high switching frequency, with considering optimum components placing. Moreover, the relation between; switching frequency, filters' size and the efficiency of the SiC based inverter have been concluded. A combination of film and aluminium dc link capacitors has been used to optimize the price – performance ratio.

This work was supported by 1002 – HIZLI DESTEK PROGRAMI Funding Program of the Scientific and Technological Research Council of Turkey (TUBITAK).

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ÖZET

Bu projede 3 faz 4-telli 2-seviye nötr noktası kenetli SiC MOSFET tabanlı Gerilim Kaynaklı Evirgeç (GKE) üzerinde çalışılmıştır. GKE, 30 KHz anahtarlama frekansında çalıştırılmış olup soğutma işlemi Alüminyum (Al) blok soğutucu kullanılarak doğal hava soğutma yolu ile yapılmıştır. Tasarlanan GKE yapısı 3 faz bağlantı imkanı sunarken kullanılan ayrık kapasitörlerin orta noktası dördüncü tel olan nötr teline bağlanmıştır. Düzgün bir şekilde tasarlanan LCL tipi filtre anahtarlama frekansında L ve LC filtreye göre daha iyi bir sönümleme karakteristiği sunduğu için tercih edilmiştir. Anahtarlama yöntemi olarak Sinüzoidal Darbe Genlik Modülasyonu (SDGM) tercih edilmiş olup açık döngü kontrol metodu kullanılmıştır. SiC temelli anahtarlama elemanları sayesinde yüksek anahtarlama frekanslarına düşük kayıplar ile çıkılabilmiş ve yüksek anahtarlama frekansı sayesinde çıkış filtresi boyutları ciddi oranda düşürülmüştür. Elektriksel büyüklüler, cihazın şebeke bağlantısı ve yenilenebilir enerji kaynakları ile beraber çalışması göz önünde bulundurularak seçilmiştir. Projede kapı sürücüsü tasarımına ayrıca önem verilmiş ve kullanılan SiC tabanlı MOSFET lerin tetiklenmesi için uygun kapı sürücüsü tasarlanmıştır. Yüksek enerji yoğunluğuna düşük hacim ve ağırlıklarda ulaşılmış olup 1 dm^3'te 2.35 kW güç üretimi yapılmış ve %98.5'tan daha yüksek bir verimliliğe ulaşılmıştır.

ABSTRACT

In this Project 3 Phase 4-Wire 2-Level neutral point clamped SiC MOSFET based Voltage Source Inverter (VSI) was carried out. VSI was operated at 30 kHz switching frequency using neutral air cooling Aluminium (Al) heat sink. While designed VSI makes 3 phase connection possible, mid-point of the capacitors allows fourth wire connection as a neutral point. Properly designed, the LCL supply filter is used instead of L and LC type filters in this work since it provides a much better suppression at the modulation frequency. As a switching method Sinusoidal Pulse Width Modulation (SPWM) method was preferred and open loop control strategy was applied. Thanks to the SiC based switching device, high switching frequency operation was realized with very low losses and also filter size was reduced dramatically because of high switching frequency. Grid connection and renewable energy source compatibility took into consideration when electrical parameters were chosen. Proper gate driver design was also cared and suitable gate driver was designed. High power density was obtained at low volume and mass. Approximately 2.35 kW power was produced in unit volume (decimetre cube) and more than %98.5 efficiency was obtained.

CHAPTER I

INTRODUCTION

1.1. System Specification

Device was designed as grid connected 3 phase 4-wire 2-level VSI type as shown in Figure 1.1. In this topology, DC source can be connected to inverter through DC – link capacitor bus. The midpoint of the DC-link was grounded to reduce voltage stress on DC bus capacitors and it creates neutral line path. Compared with L and LC type filters, LCL type filters provide many advantages such as low voltage drop due to small inductors, better harmonic attenuation performance, limited capacitor inrush current and inverter robustness under varying grid reactance so LCL type filters were chosen, as a grid interface. Measurement points such as DC link voltage sense, inverter output current measurement and output voltage sense points are used only measurement. Device has open loop control strategy since there aren't any closed loop feedback mechanisms.

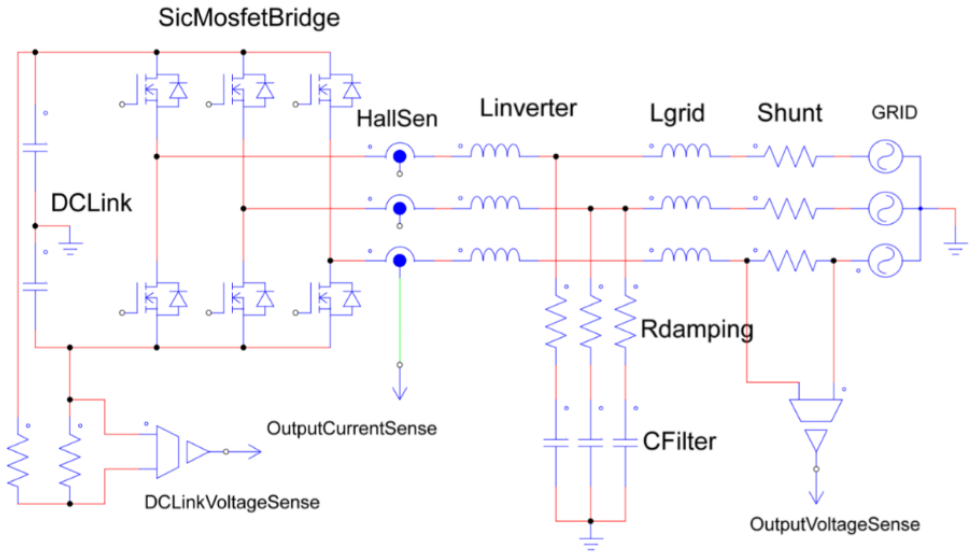

Figure 0.1. General diagram of system

Device is compatible for low voltage side connection of Δ-Y connected distribution type transformer. And also parallel connected MOSFETs enables increase power range of device.

Trace of PCB and thickness are able to carry the desired current. To avoid electromagnetic interfaces suitable suppression materials was chosen. Main electrical parameters formed according to proper selected components and manufacturer datasheets. SiC based high efficiency inverter specifications are given in Table 1.1.

Table 1. 1.System specification

Parameter	Specifications
Output Power	20 kW
Output Voltage	Three Phase 380 Vac
Output Frequency	50 Hz
Output Current	39 Ampere (25 kW) -78 Amper With Parallel Sic at 25 °C
Nominal Input Voltage	700 Vdc
Input Voltage Range	550 to 1000 Volt
Switching Frequency	20-50 kHz
Efficiency	> %98.5
Power Density	~2,35 kW/dm³
Topology	Traditional Two Level
Switching Device	Silicon Carbide Mosfet

CHAPTER II

LITERATURE REVIEW

2.1. Detailed Literature Review

In many sectors a new generation of power electronic conversion systems is being enlarged by wide-bandgap (WBG) devices. Applications are already beginning to benefit from the improved weight, size, and power capability in power converters by utilizing silicon carbide (SiC) and/or gallium nitride (GaN) switches, and numerous manufacturers are offering various types of switching devices fabricated from those two WBG semiconductors (Hudgins et al., 2003; Gil, B. ed., 2013; Jiang et al., 2012; She 2017; Burkart and Kolar, 2017; Anthon et al. 2017). Table 2.1 compares the properties of Silicon (Si) with SiC and GaN Kaplar et al. (2013). From Table 2.1, it is shown that SiC has the highest thermal conductivity, which make it the optimal choice for many application.

Table 2.1. The properties of Silicon (Si), SiC and GaN.

Property	Si	SiC	GaN
Band gap (eV)	1.1	3.0	3.4
Electron mobility (cm^2/Vs)	1400	500	1000
Thermal conductivity (W/cmK)	1.5	4.9	1.4
Breakthrough field (MV/cm)	0.25	2.5	4

There are three main physical characteristics of SiC semiconductor which makes it superior to ordinary Si devices, McBryde et al. (2010):

- Lower leakage currents. Electron-hole pairs generates much slower in SiC than in Si. This reduces the leakage current losses when the switch is off compared to Si at a given temperature.
- Increased critical breakdown strength. This implies that the device can withstand a higher voltage in the same package, or the package insulation can be reduced at the same voltage rating. Devices like Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and Junction Field Effect Transistor (JFET) can thereby be created at

blocking voltages approximately an order of magnitude higher than what is possible with Si, Elasser et al. (2002).

- A higher thermal conductivity allows for more efficient transportation of heat from the device. Additionally, the on-state resistance through the switch is lower, causing decreased conducting losses.

Moreover, in conventional bipolar Si switches, e.g. insulated-gate bipolar transistor (IGBT), the switching frequency is limited by the time required for the plasma in the drift region to establish and be removed. For unipolar SiC devices this limit does not apply, allowing significantly higher switching frequencies, Anthony et al. (2014).

SiC has a wide bandgap of 3 electronvolt (eV) and a much higher thermal conductivity compared to silicon. SiC based MOSFETs are most suited for high breakdown, high power applications that operate at high frequency as shown in Figure 2.1, Infineon (2019). Compared to silicon, the device parameters such as; the resistance between drain and source during on state ($R_{DS(on)}$) change less with temperature. This allowing extra performance to be delivered.

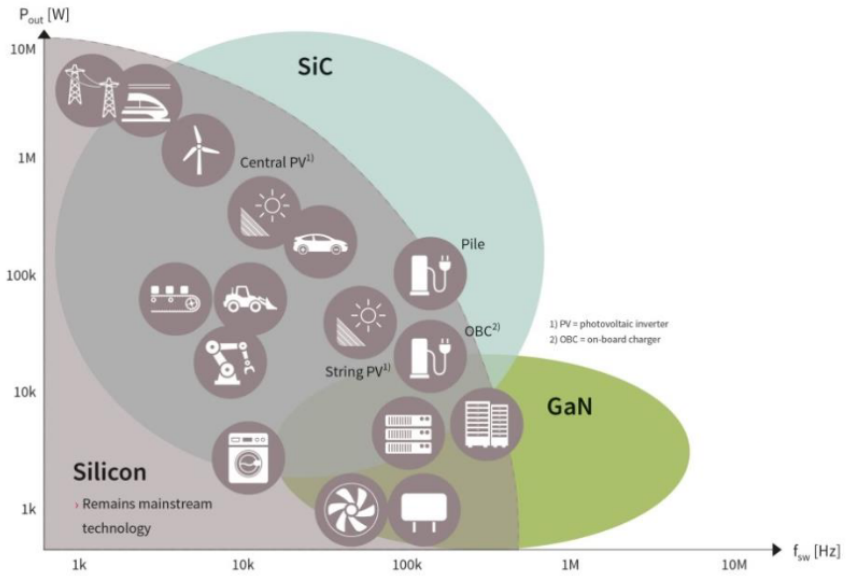

Figure 0.1. The range of frequency and power for Si, SiC and GaN with different applications

The need for high power density, power conversion is expected to increase as renewable energy interfacing requirements continue to accelerate. Converters can be integrated within the host device they are intended to support, as converter power density increases to higher levels. These unprecedented levels of power density are supported in part by the current commercial availability of SiC power switches and drivers. This particular combination of potential high-speed, high-voltage, and high-temperature behavior associated to SiC, makes it very attractive for applications in power electronics that require these behavior aspects, such as for three phase grid connected Photovoltaic (PV) solar inverter with high rated power.

As it has been studied in my published papers (Jaalam N. et al. 2017; Eid B.M et al. 2016) and my PhD thesis Eid B.M (2016) the inverter is playing the main role in controlling the PV solar systems with many ancillary services associated with it nowadays. Figure 2.2, from Eid B.M (2016) shows one of the ancillary services, which is injecting reactive power to contribute to the stability of the public grid.

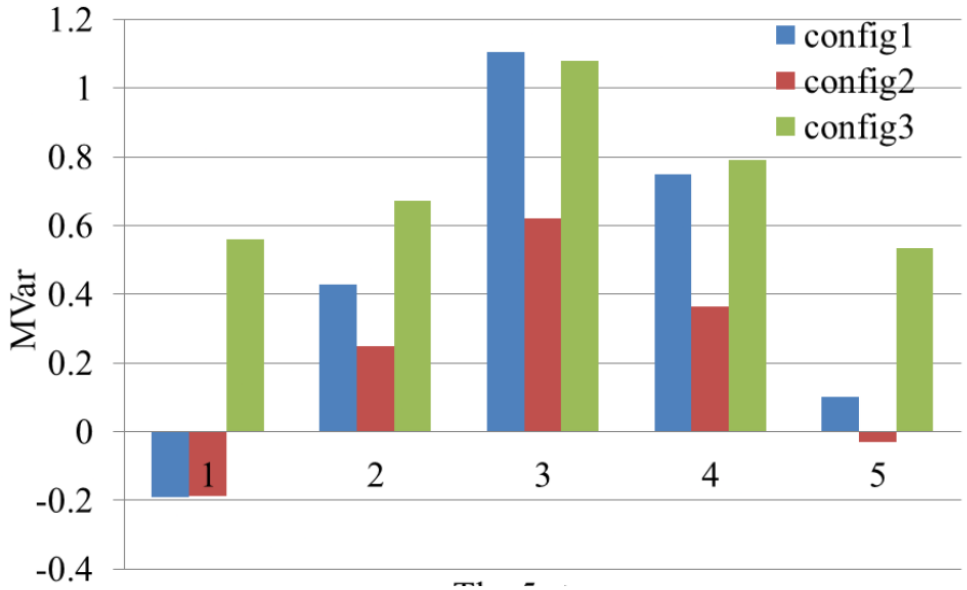

Figure 0.2. Reactive power dispatched from an inverter in the three different configurations, shows some ancillary services of the three phase inverters.

In the solar energy market the, PV converters, especially the three phase string inverters have been under rapid growth. A three-phase string inverter is a two-stage inverter connected to three-phase utility grid without a transformer SMA (2019), ABB (2019). The typical power ratings of three-phase string inverters are from 10 to 100 kW. The SiC based PV string inverters have been under research and development recently because of the technology maturity of 1200 V SiC devices. Although it is well accepted that SiC devices have significant advantages over Si devices in terms of switching speed, switching loss, and temperature stability, (Jiang et al., 2012; She 2017), many technical challenges have to be tackled to transfer from the device level advantages to system level benefits.

The common practice to develop a SiC-based PV inverter nowadays is to directly replace the Si switches with SiC switches in conventional topologies. In Deboy et al. (2011), SiC JFETs were used to substitute Si IGBT in a 17-kW three-phase string inverter based on the three-level T-type (3LT2) topology. Peak efficiency has been increased from 98.2% to 98.8%. However, using a SiC device without increasing power density is not beneficial to lower the system level cost, which poses a major disadvantage in the highly competitive PV inverter markets. SiC PV inverters presented in (Burkart and Kolar, 2017; Anthon et al. 2017; Gurpinar and Castellazzi, 2016; Kolar and Rurkart, 2015) can achieve better power density by increasing the switching frequency so that the components cost can be reduced. In Mookken et al. (2014), an air-cooled 50-kW three-phase two-stage all SiC PV inverter was presented. The dc–dc stage is an interleaved boost converter switching at 75 kHz and the dc–ac stage is a 3LT2 inverter switching at 50 kHz. The power density of this PV inverter is 1 kW/kg, which is about three times higher than that of conventional Si-based PV inverters. However, researchers in (Gurpinar and Castellazzi, 2016; Kolar and Rurkart, 2015) also showed that the approach of increment in power density and efficiency by just replacing the switching devices has its limitations. The main reason is that while increasing the switching frequency, the current ripple of the switching frequency on inductors will generate additional specific power loss and in order to dissipate this power loss the inductors have to be oversized.

In this project the design for a three phase inverter using SiC MOSFET has been implemented under high switching frequency and high power capability. The variation of switching frequency in parallel with variation of filtering component’s size in order to investigate the incremental of the power density of the system without compromising the efficiency.

CHAPTER III

METHODS AND MATERIALS

3.1. Power Board Design Criteria

When designing a printed circuit board there are many design criteria have to be followed;

- Based on the current passing in the PCB the thickness and the width of the tracks of the board have to be defined carefully. In our project the standard thickness of the board has been chosen for the cost and the availability issue which is 1.6 mm for the board and 1 oz for the copper thickness. However, for the width of the tracks, base on the well known equation of the track current passing capability ($I = v*A/(L* \rho)$) with this way wider track on the DC positive and negative Busbars can be obtained.
- Even though the rated current of the SiC MOSFET LSIC1MO120E0080 that we used in this project was 39 A it is very important to operate within the temperature limits otherwise the max possible DC current will drop 40% (only 60% of the normal value).
- In the design we found that the DC current has to pass first via the DC link capacitors to charge them then after few cms it goes to the SiC Mosfet. This will generate a voltage with better sine wave.
- In the design we developed, the gate drive circuit is so close to the SiC Mosfet in order to avoid gate ringing, parasitic inductance and to keep the frequency distortion as low as possible. Moreover all the distances between all SiC Mosfets and the gate drive circuits are the same to have the correct required signals pulsing each SiC mosfet.
- If circuit board contains both power and signal circuits, 4 or more layers have to be chosen in the PCB. The layers in the terminals will be used for Power and the two layers in the middle will be for the signal circuits.
- If there is no chance to make multilayer board (4 layers) separated boards for signal and power circuits can be developed. In this project because of the budget and availability limitations we used only two separated layers.
- Thermal management should be considered before designing the board and proper heatsinks have to be chosen. In case of the limitation of the space the heatsinks size can be reduced and a fan has to be added.
- If there is a snubber circuit on the board, snubber circuit's components have to properly placed in board to prevent voltage sparks, this will eliminate overshoot. I this project the snubber capacitors place closed to the drain and source terminal of each half bridge legs.

- The footprint of each component has to be chosen properly. In this project the datasheet of each component has been studied and the dimensions have been placed inside a software to generate the final shape of the PCB board.
- Gate resistors in the gate drive circuit should be well calculated and it has to be in good quality in order to keep the circuit stable. In this case the Melf resistor has been chosen in this project.
- Bleeding resistors should be connected in parallel with the DC link capacitors, in order to discharge the capacitors for safety reasons.
- There has to be a proper isolation between high voltage and low voltage areas. Such as the DC and AC power circuits and the gate drive circuit. In this project different separate circuits have been used.
- There should be some test points for prototype boards, to facilite measurement.

3.2. Optimum DC Link Voltage

DC link voltage (Vdc) has effects on some features of the inverter, such as efficiency and high frequency current ripple on the filter inductor. For the same output filter inductance value, higher DC link voltage results in increase of the switching frequency current ripple, which increase magnetic losses in the inductor and current harmonic distortion at the switching frequency. The value of DC link voltage which is regulated by maximum power point tracking (MPPT) technique by using the converter. The input of the inverter is kept constant in the entire range of operation, no matter the amount of PV power. VSI is supposed to transfer all the power from MPPT converter, to grid and by keeping the value of the DC link constant, this duty is accomplished. As the solar power increases, power output of the MPPT converter increases, and this condition results in the increase of the DC link voltage. As the Vdc increases, the modulation index (M) decreases. Modulation index M directly affects on maximum output phase voltage with DC bus voltage as given in 3.1. According to the given formula in 3.1. V denotes RMS output voltage and Vdc represent DC bus voltage.

$$M = \frac{2\sqrt{2}}{\sqrt{3}} \frac{V}{V_{dc}} \tag{3.1}$$

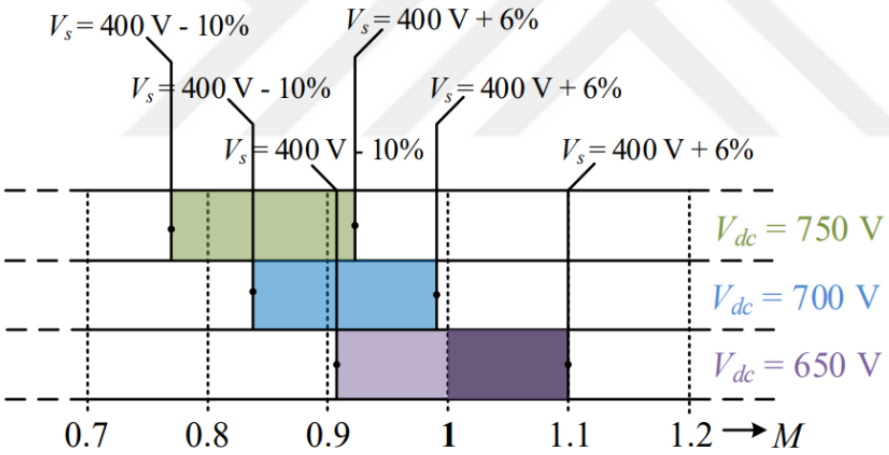

Figure 0.1. Range of variation of modulation index M for different fixed values of DC bus voltage and for connected 400 V l-to-l, 50 Hz grid voltage variations upper and lower limits as 400 V +6% -10% as specified in IEC 60038 2002-07

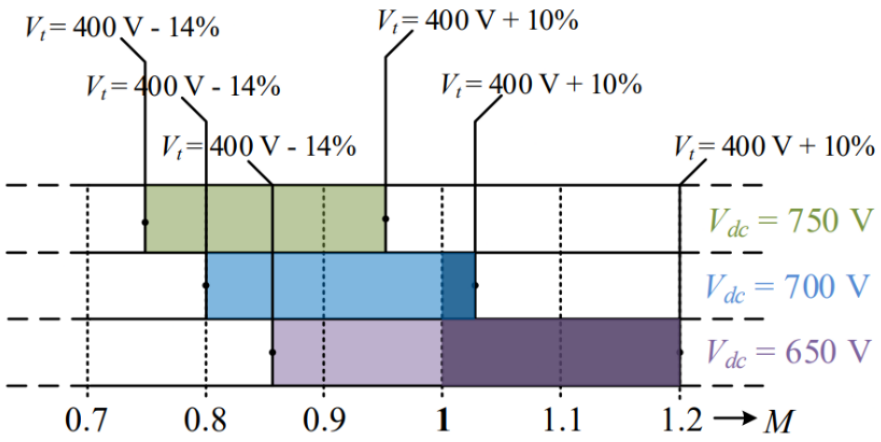

Figure 0.2. Range of variation of modulation index M for different fixed values of DC bus voltage and for connected 400 V l-to-l, 50 Hz grid voltage variations upper and lower limits as 400 V +10% -14% as specified in IEC 60038 2002-07

According to Figures 3.1 and 3.2 it can be understood that optimum value for DC link voltage is around 700 V. For the supply side voltage upper and lower band limits, inverter does not goes into overmodulation, which causes low order harmonics. For the utilization voltage range, inverter works in slightly over-modulated at the upper band limit, which is acceptable. For 650 V DC bus voltage, inverter works highly over-modulated at the upper band limits of both supply side voltage and utilization voltage, which is unacceptable since low order harmonics grow dramatically. In case of 750 V DC link voltage, inverter does not operate into over-modulation in any case, and the modulation index M, is too low, which increases losses for the same switching frequency and same output filter. By considering these reasons listed above. DC link voltage is designated as 700 V.

3.3. Optimum Switching Frequency

For many modulation techniques, such as Sinousidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM), as the switching frequency increases, frequency of high order harmonics (which are also known as side-band harmonics) occurring at the both sides of switching frequency and its' multiplies, also increases. Becuase of that, output filter corner frequency, in other words resonant frequency of LCL filter, can be set to a higher value in order to reduce the volume of passive components. However, increasing switching frequency has a drawback in terms of losses. As the switching frequency increases, switching loss occurring in power semiconductors proportionally increases with the frequency. Traditional Si based power semiconductors, such as IGBT, has significantly larger turn-on, turnoff times with respect to SiC based power semiconductor. Due to this, with the emergence of SiC power MOSFETs, switching frequency can be increased more, in comparison to IGBT switching frequency, for the same power rating of the inverter and for the same switching loss. But, benefits of increasing switching frequency, in terms of lowering the size of passive components, start to saturate at one point in the control stability point of view. Reducing inductor component of output filter causes stability problems, since voltage and phase difference between inverter output voltage and grid voltage is necessary to control power flow to grid. Low order voltage harmonics in the grid cause low order current flows, despite control circuitry current loop attenuation. Because of this reasons, output filter inductance has a minimum value which has been shown in output filter design section, so that increasing switching frequency too much has no advantage after one point. In order to find optimum switching frequency, 10 kHz switching

frequency has almost no advantage in terms of switching losses and LCL filter size which needs to be increased significantly. LCL filter copper loss increases dramatically, in order to have the same switching current ripple. In the case of 30 kHz switching frequency, LCL filter volume reduction is significant in comparesion to 20 kHz switching frequency, in addition, switching loss of SiC MOSFETs starts to be a considerable amount. Also, because of the mentioned control loop stability problems, due to insufficient impedance between inverter output and grid voltage, 30 kHz switching frequency is not considered big engouph to reduce the filter size.

3.4. DC Bus Capacitance Calculation and Capacitor Selection

When choosing DC link capacitor of the three-phase grid connected inverter, some parameters such as DC link capacitance, rated DC link voltage, capacitor ripple current and life time of capacitor need to be considered. The capacitance of DC link capacitance is very improtant, it recduces the voltage ripple generated due to high frequency. And the DC link capacitance is typically selected to meet the design criteria of up to 2% voltage ripple on the DC link. Maximum power transfer from DC bus to grid in a single switching period, is given in the following formula.

$$\Delta W = T \times Pmax \tag{3.2}$$

According to maximum power transfer, DC link capacitance, DC link voltage and ripple voltage on the DC link are given as;

$$\Delta V_{dc} = \frac{\Delta W}{V_{dc} x C_{min}} \tag{3.3}$$

Minimum DC link capacitance can be calculated, in order to meet the required ripple at the maximum power transferring to grid as;

$$C_{min} = \frac{T x Pmax}{V_{dc} x \Delta V_{dc}} \tag{3.4}$$

Even though installed PV array power rating is 20kW, inverter is designed to transfer 30 kW power to grid. Because of that, calculations made for 30 kW maximum power. For 30 kW Pmax, 30 kHz switching frequency, 700 V DC link voltage and 1% ΔVdc, Cmin is calculated as 480 uF. Other criteria to select DC bus capacitor, are equivalent series inductor, ESL, and equivalent series resistance, ESR, value of the capacitor. ESR value is critical in a way that determining ripple current capacity of the capacitor. Lower ESR means higher ripple current capacity, and

less thermal stress on the capacitor, which increase the life time of the capacitor. ESL value of capacitor is important, in terms of voltage spikes on SiC MOSFETs, during turn off. By considering all the reasons listed above, The Table 3.1 shows the capacitor design for film and Electrolytic type.

Table 3.1. Capacitor Selection Table

Specification	C3D2H226JB00C00 Film	K055002210PM0E040 Electrolytic
Type	Metallized Polypropylene	Electrolytic
Irms (ripple current)	10 Amper	950mAmper
ESR(Equivalent Series Resistance)	5 m ohm	455m ohm
Capacity	22uF	220uF
Voltage	500 Volt DC	500 Volt DC
Life cycle	100000 hour at 70 Degree	5000 hour at 105 Degree
Cost	10 times more expensive for the same capactance	cheaper for the same capactance

For 480 uF 1000 volt DC link system can be made by the combination of film and electrolytic capacitors in series and parallel. This make us able to gain the features of both capacitors, such as:

- The high equivalent series resistance (ESR) value of electrolytic capacitor (which is not preferable) will be decreased so the life time will be increased.
- The not prefered ripple current which is high in the electrolytic capacitor will be mitigated by using the film capacitor in parallel.
- Because of Low capacity of film capacitor, if we have used just film capacitors then we have to use 86 film capacitor to reach 480 uf, and by combining the film capacitor with the electrolytic capacitor we can reduce the required number of capacitors in the board so we can save the space in the board for orther components and product smaller PCB.
- High capacitance value of electrolytic capacitor will help reducing the cost of the required DC link capacitors.

To reach 440 uFcapacitance value 2 electrolytic capacitor was connected in series with this way 1000V DC voltage level was obtained. As a general DC-link capacitor connection scheme 220µF Al electrolityic capacitor was connected in series and four group was

obtained then these groups connected as paralel with the same way 22μF film capacitors were connected. With this way total 484uF DC-link capacitance value was obtained as shown in Figure 3.1.

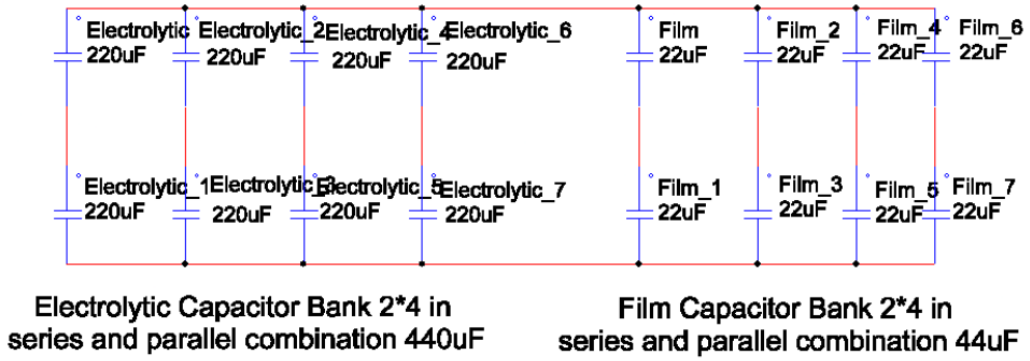

Figure 0.3. Capacitor connection scheme

3.5. Output Filter Design and Inductor Design

As an output filter LCL filter was used. It is obvious that LCL filter is a third-order filter and has common usage and better performance than L type and LC type filter since it has smaller inductance and capacitance value and shows better harmonic attenuation performance. Furthermore, the voltage drop across the filter is less than the other types. Three phase four-wire VSI filter is illustrated in Figure 3.2.

One of the key benefits of using SiC MOSFETs is the ability to increase the switching frequency of the power stage significantly versus traditional Si-based switching elements. This increased switching frequency has a direct impact on the inverter's output filter resonant design, which needs to be accounted for.

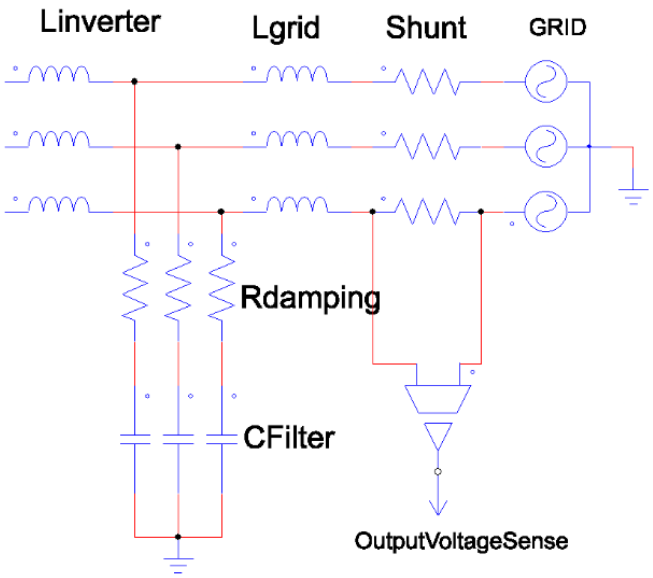

Figure 0.4. 3 Phase LCL filter general scheme

To ensure that the filter is designed correctly around switching frequency, common mathematical model was used in this design. The primary component is the inverter inductor, or L inv, which can be derived using eq. 3.5. According to our design parameters Linv was found as 267 µF in Eq. 3.6.

$$L_{inv} = \frac{V_{dc}}{8 \times f_{sw} \times I_{grid\_rated} \times \%ripple} \tag{3.5}$$

$$L_{inv} = \frac{1000}{8 \times 30kHz \times 39A \times \%40} = 267\mu H \tag{3.6}$$

The sizing of the primary filter capacitor is calculated according to the eauation 3.7. And calculated filter capacitor value is given in 3.8.

$$C_f = \frac{\%x \times Q_{rated}}{2 \times \pi \times 50Hz \times \frac{380^2}{\sqrt{3}^2}} \tag{3.7}$$

$$C_f = \frac{\%5 \times \frac{20kW}{3}}{2 \times \pi \times 50Hz \times \frac{380^2}{\sqrt{3}^2}} = 22\mu F \tag{3.8}$$

Determining attenuation factor which is defining as between the allowable ripple in grid inductor and the inverter inductor can be described as a first step in filter design. This factor needs to be minimized while designing a stable and cost effective filter. Attenuation factor, symbolized as r value, defines the ratio between the two inductors, and can be calculated using Eq. 3.9.

$$I_{att} = \frac{1}{|1 + r \times (1 - L_{inv} \times C_f \times (2 \times \pi \times f_{sw})^2 \times x)|} \times 100 \tag{3.9}$$

To obtain an attenuation factor of 10%, and using the earlier derived values, the value of r can be evaluated by rewritingaccording to the 3.10.

$$r = \left| \frac{\frac{1}{\%10} - 1}{1 - 267\mu H \times 22\mu F \times (2 \times \pi \times 30kHz)^2 \times \%5} \right| = \sim\%5.4 \tag{3.10}$$

The final value of L grid is then;

$$L_{grid} = r \times L_{inv} \tag{3.11}$$

$$L_{grid} = \sim\%5.4 \times 267\mu H = 14.4\mu H \tag{3.12}$$

The filter design can be validated by determining its resonant frequency (Fres). A good criteria for ensuring a stable Fres is an order of magnitude above the line frequency and less than half the switching frequency. This criteria solves upper and lower harmonic spectrum problems. The resonant frequency of the filter is defined as 3.13. Calculated Fres is given in 3.14.

$$F_{res} = \frac{\frac{1}{\sqrt{C_f \times \frac{L_{grid} \times L_{inv}}{L_{grid} + L_{inv}}}}}{2 \times \pi} \tag{3.13}$$

$$F_{res} = \frac{\frac{1}{\sqrt{22uF \times \frac{14.4\mu H \times 267uH}{14.4\mu H + 267uH}}}}{2 \times \pi} = 9.179kHz \quad (3.14)$$

The remaining calculation is the passive damping resistor value that must be used to avoid oscillation. Generally, a damping resistor at the same relative order of magnitude of the Cf impedance at resonance frequency. This impedance is easily derived using 3.15.

$$R_d = \frac{1}{6 \times \pi \times F_{res} \times C_f} \quad (3.15)$$

$$R_d = \frac{1}{6 \times \pi \times 9.179kHz \times 22uF} = 0.262ohm \quad (3.17)$$

Output filter is one of the major contributors to the size and weight of a solar inverter, and must be ensured that the individual components are correctly sized. High system switching speed provided by the SiC MOSFETs and thanks to the this feature filter size can be decreased dramatically. According to the simplified equation which is given in 3.18 the inductance of an inductor, has a lineer proportion with permeability, inductor cross sectional area with a number of turns. Both have a direct effect on the size of the component.

$$L = \frac{0.4 \times \pi \times \mu \times N^2 \times A \times 10^{-2}}{l} \quad (3.18)$$

Inductor size can be determined using 3.18 and abbreviations descriptions are given in below;

- μ is core permeability
- N is the number of turns
- A is the cross sectional area
- l is the mean magnetic path length

A valid core material and subsequent permeability selection is the most crucial points to design proper inductance. The core manufacturers typically has a wide range of suitable materials with selection table according to the target inductance value and the inductor current. For this design, the nominal inductor current (with an overload factor of 105%) is defined as 3.19.

$$I_{ind\_nom} = \frac{KVA_{out} \times \%105}{\sqrt{3}V_{grid}} \quad (3.19)$$

$$I_{ind\_nom} = \frac{20kVA \times \%105}{\sqrt{3} \times 380} = 31.9\ Amper \tag{3.20}$$

Using a selection guide for a toroidal inductor core manufacturer, at 267 μH, the core permeability is found as 20. The core also provides a value for the inductance factor, AL , which enables a quick path to selecting the number of turns.

$$N = \sqrt{\frac{L \times 10^3}{A_L}} \tag{3.21}$$

$$N = \sqrt{\frac{267 \times 10^3}{49}} = 74 \tag{3.22}$$

One last piece of information required for the inductor design is the winding wire size. This size is easily computed using the nominal inductor current rating. Using copper, with a current carrying density of 4 A/mm, this inductor requires a cross sectional area of:

$$A_w = \frac{I_{ind\_nom}}{4} = \frac{31.9}{4} = 7.97mm^2 \tag{3.23}$$

This area is an equivalent to American Wire Gauge #8, which has a cross sectional area of 8.37 mm2 . With the flat 8 AWG winding, the total length of each winding is determined to be 68 mm. At this point, the DC resistance of the inductor can be calculated using Pouillet's Law:

$$R_{DC} = p\frac{l}{A} \tag{3.24}$$

$$R_{DC} = (10^{-9} \times 17) \times \frac{74 \times 68\ mm \times 10^{-3}}{7.97mm^2 \times 10^{-6}} = 0.0107ohm \tag{3.25}$$

To determine the AC resistance, first skin depth is calculated at the inverter switching frequency according to the 3.26. Measured skin depth is given in 3.27.

$$S_d = 1000 \times \sqrt{\frac{p}{\pi \times f_{sw} \times \mu_0}} \tag{3.26}$$

$$S_d = 1000 \times \sqrt{\frac{10^{-9} \times 17}{\pi \times 30kHz \times 4 \times \pi \times 10^{-7}}} = 0.37mm \quad (3.27)$$

Then RAC is determined by using RDC, Sd , and Ss , which is the equivalent square conductor width.

$$R_{AC} = R_{DC} \times \frac{1}{2} \times \left(\frac{S_s}{S_d}\right) \times \left(\frac{sinh\left(\frac{S_s}{S_d}\right) + sin\left(\frac{S_s}{S_d}\right)}{cosh\left(\frac{S_s}{S_d}\right) - cos\left(\frac{S_s}{S_d}\right)}\right) = 0.033ohm \quad (3.28)$$

This determination of RAC helps determine total system losses.

3.6. SiC MOSFET Selection

The LSIC1MO120E0080 part number silicon carbide MOSFET from littelfuse company has been chosen for this project. Chosen MOSFET specifications are given in Table 3.2. Features and application area of this switch:

- Optimized for highfrequency, high-efficiency applications
- Extremely low gate charge and output capacitance
- Low gate resistance for high-frequency switching
- Normally-off operation at all temperatures
- Ultra-low on-resistance
- High-frequency applications
- Solar Inverters
- Switch Mode Power Supplies
- UPS
- Motor Drives
- High Voltage DC/DC Converters
- Battery Chargers
- Induction Heating

Table 3.2. SiC MOSFET specifications

Characteristics	Value
Drain Source Voltage	1200 Volt
Drain Source Open Resistance	80 mOhm
Continuous Drain Current	39 Amper at 25℃
Pulsed Drain Current	80 Amper at 25℃
Power Dissipation	179 W
Operating Junction Temperature	-55 to 155℃
Gate-source Voltage	-5 to 20 Volt

3.7. Gate Driver Selection and Dedicated Gate Driver Board

TLP152 part number photocouple was chosen as gate driver from Toshiba brand, this gate driver will create signal isolation between control and power circuit. General charachteristic of TLP152 is given in Table 3.3.

Table 3.3. TLP152 Gate driver charcteristics

Characteristics	Value
Output peak current	±2.5 A (max)
Operating temperature	- 40 to 100 ℃
Supply current	3.0 mA (max)
Supply voltage	10 to 30 V
Threshold input current	7.5 mA (max)
Isolation voltage	3750 Vrms (min)

SiC Mosfets can be driven at very high frequencies and gate resistor requirement is very low according to the traditional ones. In this inverter gate resistors is 2 ohm and the total gate to source voltage is +20/-5. By making rough calculation for 2 ohm gate resistance we need 25/2=12.5 amper gate current driver so we can choose non isolated ultra fast 14 amper gate driver from IXDN brand called as IXDN614si. General charachteristic of IXDN614si is given in Table 3.4.

Table 3.4. IXDN 614 Gate driver specification

Characteristics	Value
Output peak current	±14 A (max)
Operating temperature	-55 to 150 ℃
Supply current	2.0 mA (max)
Supply voltage	0 to 40 V
Threshold input current	10 uA (max)
Isolation voltage	0

PCB board have been designed with combination of this gate drivers and it has isolated DC/DC converter to supply gate drivers, gate resistances and decoupling capacitors, also it has double layer circuit. Detailed schematic is given in Figure 3.5. In order to give more detail layout and 3D modelling view are given in Figure 3.6. and 3.7. respectively.

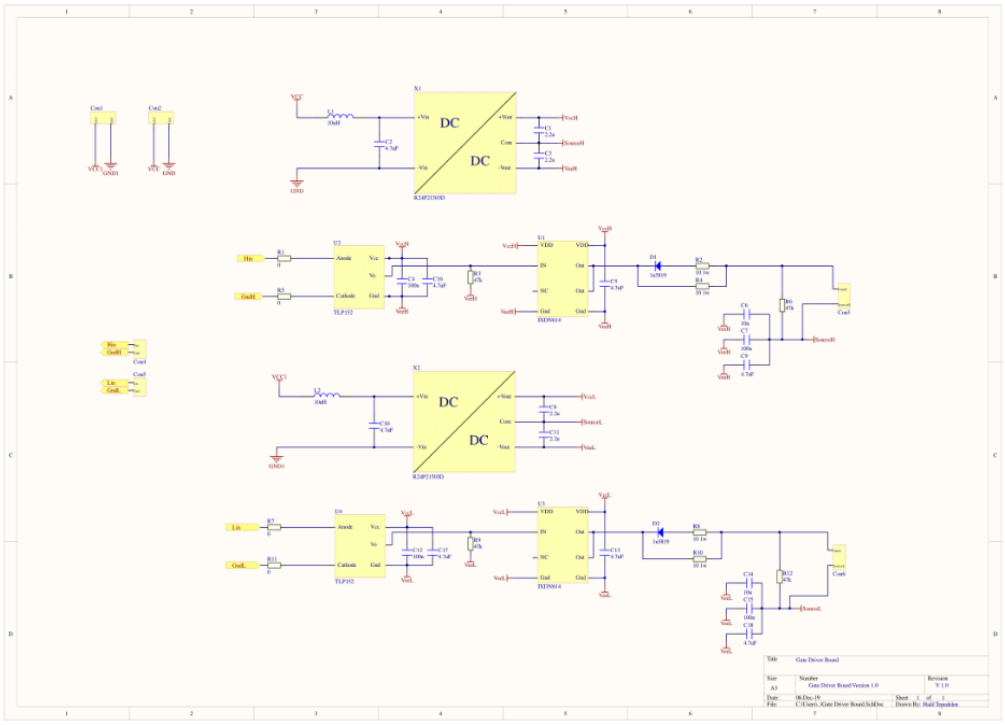

Figure 0.5. Schematic drawing of gate driver board

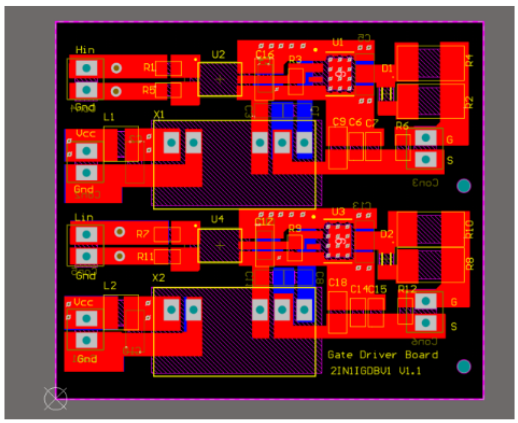

Figure 0.6. Gate driver layout drawing

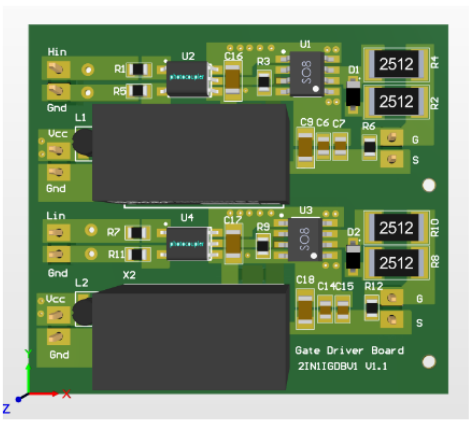

Figure 0.7. Gate driver 3D view

For supplying each gate driver we provided rkz-122005d part number DC/DC converter from RECOM it has 2W of continious power and 3kV isolation voltage.

3.8. Theoretical Loss Calculation

The primary source of lost efficiency in any inverter is going to be a result of the losses incurred in the switching devices. These losses are broken into three categories for each device:

• Conduction loss: When the device is on and conducting normally

• Switching loss: When the device is switching between states

• Diode conduction loss: Related to voltage drop and current when in conduction Each of these are dictated by their own equation, and can be determined from the device data sheet and design parameters that have already been set. Conduction loss is driven by the on-time of the FET is given in Eq. 3.29.

$$P_{cond\_lost} = \frac{1}{T}\int_0^T V_{ce}(t) \times I_c(t) \times D_D(t)dt \tag{3.29}$$

$$P_{cond\_lost} = \frac{1}{T}\int_0^T 3.12 \times 39 \times 0.9dt \tag{3.30}$$

where

• Vce is the conduction voltage drop

• Ic is the conduction current

• DD is the duty cycle

• T represents one modulation cycle

Switching loss is determined according to the switching energy of the device and the switching voltage at the selected test point. To determine the value of the switching energy, designed external gate resistor value from the device data sheet was used. The remainder of the values needed were determined earlier from the design phase. Switching loss is calculated by using 3.31.

$$P_{sw\_loss} = \frac{(E_{on} + E_{off}) \times I_{peak} \times f_{sw} \times V_{DC}}{\pi \times I_{avg} \times V_{nom}} \tag{3.31}$$

$$P_{sw\_loss} = \frac{(280\mu j + 80\mu j) \times 39 \times 30kHz \times 350}{\pi \times 39 \times 1000} = 1.203W\ Per\ Switch \tag{3.32}$$

Figure 3.8. shows an example of the graph is used to extract the switching energy values from the device data sheet for an LSIC1MO120E0080 SiC MOSFET. Even at this stage, it is easy to see that higher electron mobility in SiC is reduced switching loss.

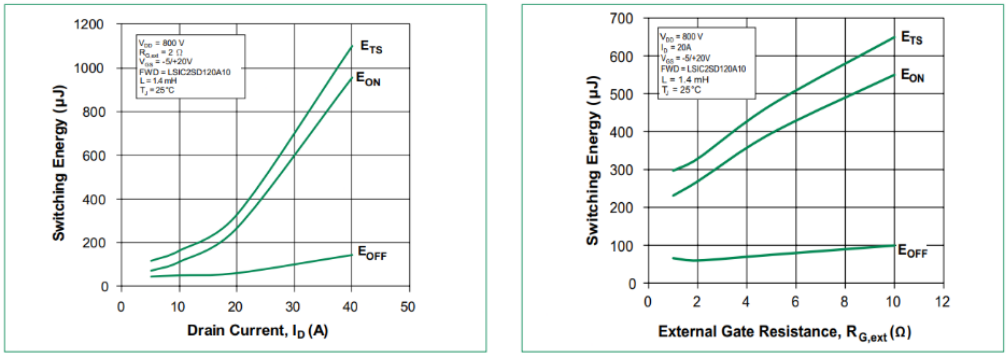

Figure 0.8. Switching Energy vs Gate Resistance and Drain Current for LSIC1MO120E0080

The diode conduction loss is similarly calculated using known values:

$$P_{sw\_diode} = \frac{1}{T}\int_0^T V_f(t) \times I_f(t) \times D_d(t)dt \tag{3.33}$$

where ;

• Vf is the voltage drop

• If is the diode current

• DD is the duty cycle

• T represents one modulation cycle

Inductor losses can be calculate according to the equation 3.34. Calculated loss value is given in 3.35.

$$P_{ind\_loss} = I^2_{ind\_ac\_rms} \times R_{DC} \times I^2_{ind\_ripple\_rms} \times R_{AC} \tag{3.34}$$

$$P_{ind\_loss} = 1 \times 0.0107 + 31.9^2 \times 0.033 = 11.1W \tag{3.35}$$

Total İnverter losses can be calculated using 3.36.

$$P_{total\_loss} = 6 \times P_{total\_sic\_mosfet\_loss} + 3 \times P_{ind\_loss} \tag{3.36}$$

And theoretical inverter efficiency can be evaluated like below.

Table 3.5. Theoritical loss calculation

Conduction Loss	4.095×6= 24.57W
Switching Loss	1.203W×6= $7.21W$
Diode Loss	2.1W×6= 12.6W
Inductor Loss	11.1W×3= 33.3W
TOTAL LOSS	77.68W

$$Efficiency_{inverter} = \frac{P_{Out}}{P_{Out} + P_{loss\_total}} \tag{3.37}$$

$$Efficiency_{inverter} = \frac{20kW}{20kW + 77.68W} = \%99.6 \tag{3.38}$$

CHAPTER IV

RESULTS AND CONCLUSIONS

4.1. Implemented Device and Test Results

A 20 kW SiC based high power density inverter is designed according to the specifications given in Chapter 3. The developed VSI device is shown in Figure 4.1 tested in Hasan Kalyoncu University Labs. This board covers DC – link capacitors, gate drivers, LCL filter, SiC MOSFET, and heat sink. Implemented device was tested under laboratory conditions and results are given in this section.

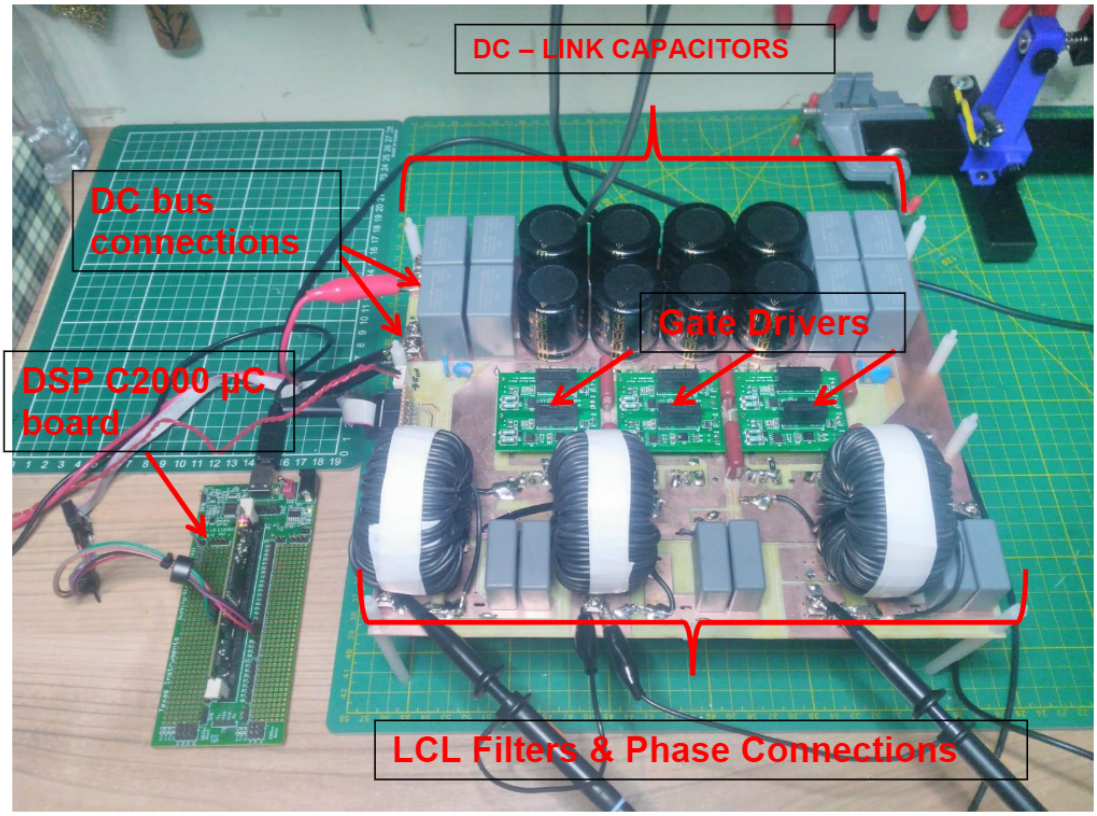

Figure 0.1. Developed SiC based VSI

Developed SiC based VSI is produced according to the schematic drawing as given in Figure 4.2. This schematic was drawn by project team using Altium Software (by using valid student version license). MOSFETS and heat sinks are clearly seen from the schematic drawing given in Figure 4.2. However, on the board placement to obtain better cooling performance and to use board area efficiently MOSFETs and heat sink placed to bottom layer of PCB.

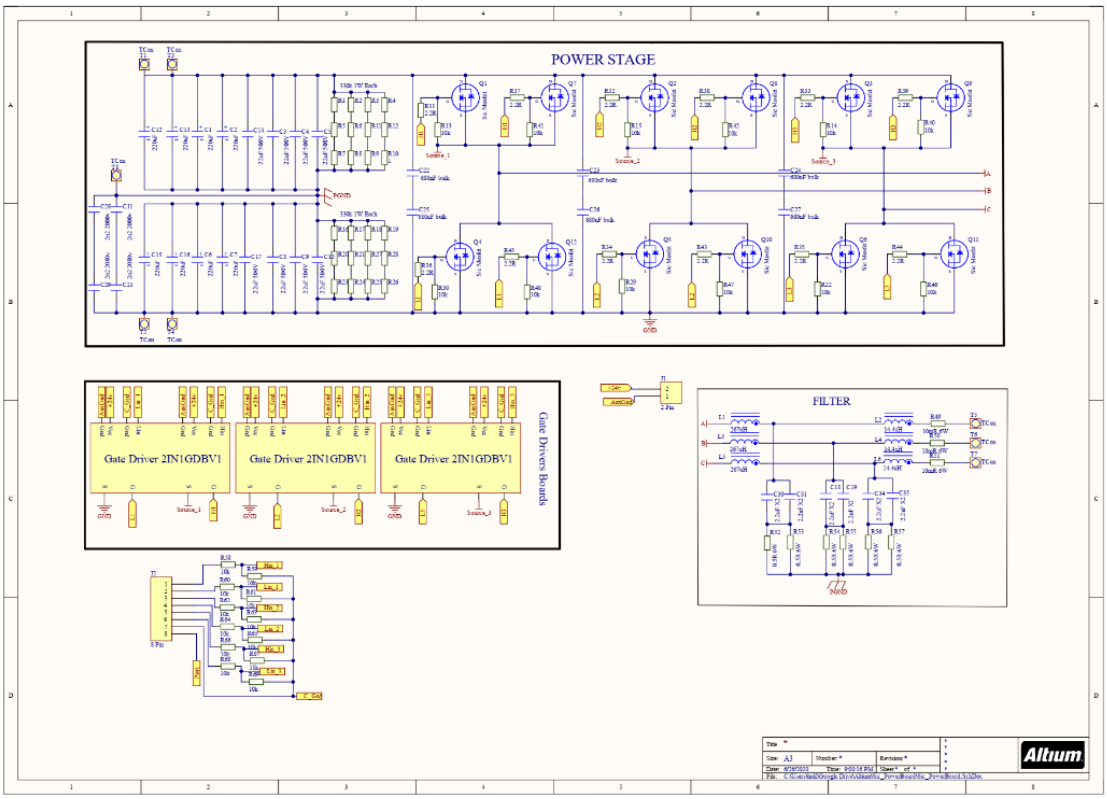

Figure 0.2. Schematic drawing of SiC based VSI

To analyse performance of the VSI, UNI-T 2102CEX 2 channel 100 MHz digital oscilloscope and Fluke 435-II power quality analyser were used. Since UNI-T 2102CEX has only two channel, 3 phase couldn't be observed simultaneously on oscilloscope screen. However two phase pairs were measured separately such as phase AB and phase BC etc. In lab condition only we could produce 30V and 60V DC from power supply so DC bus capacitor charged up to these values. Output voltage was measured using test setup as shown in Figure 4.3. DC power supply was set to 60V DC and DC-link capacitors were charged to this value then at 1 modulation index tests were carried out. Oscilloscope screen which is seen in Figure 4.3. shows phase to phase output

voltage of SiC based VSI. At that time taken screen shot of the voltage waveform is given in Figure 4.4.

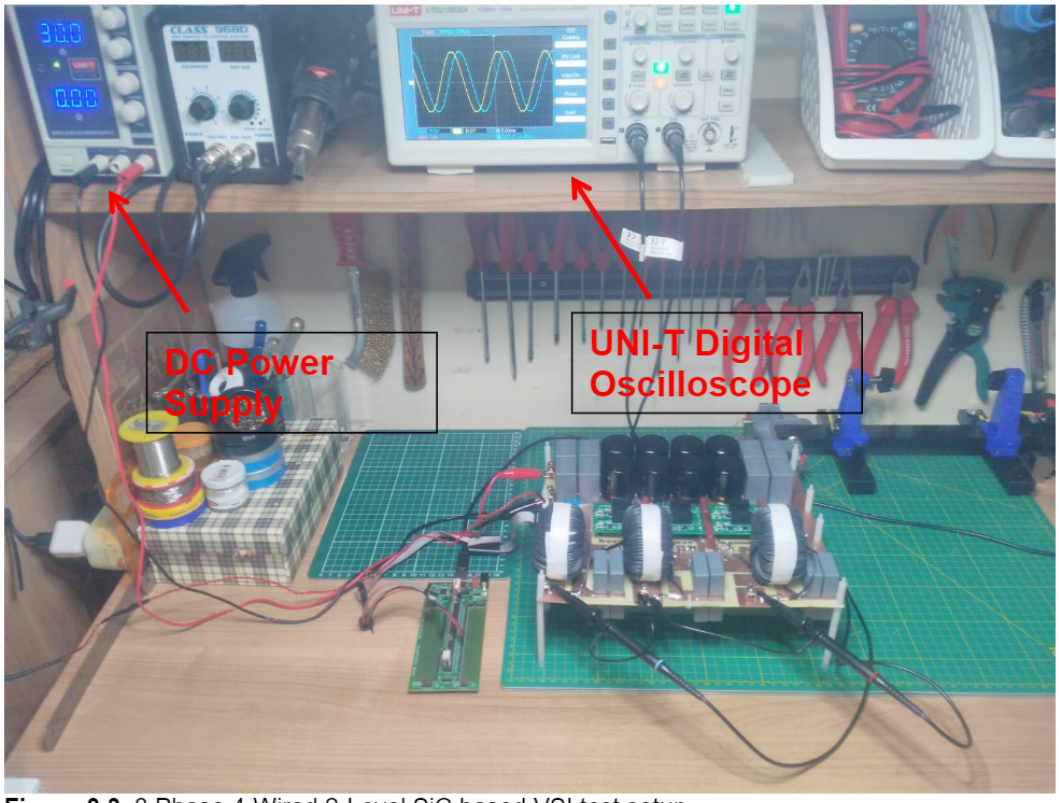

Figure 0.3. 3 Phase 4-Wired 2-Level SiC based VSI test setup

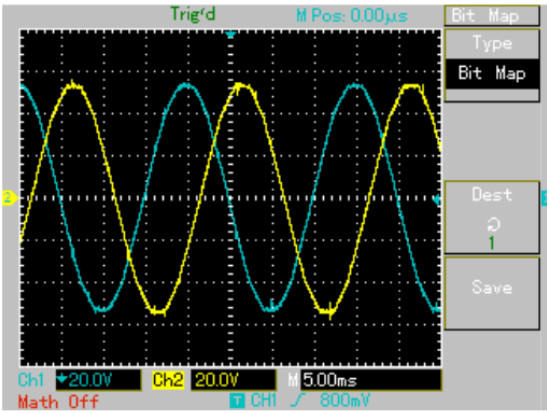

Figure 0.4. Oscilloscope screen shot of the output voltage @ 60 V DC-link

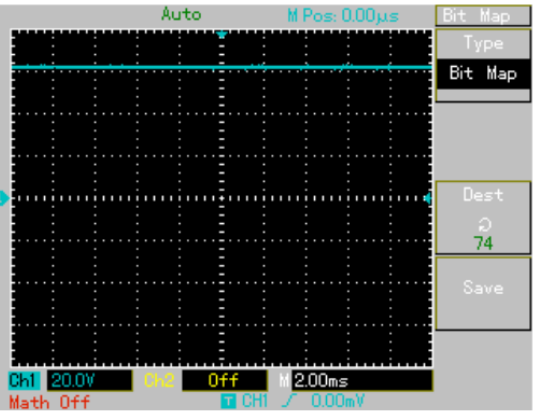

Figure 0.5. DC-link voltage measurement

When DC-link was measured as 60V, output voltage peak value was measured as 58.5V it means that we achieved close to 1 modulation index. Using Fluke 476-FC measurement was repeated and DC link voltage was decreased to the 30V DC. Fluke 476-FC was measured 3 phase RMS output voltage simultaneously and it gave us an oscilloscopic waveform picture as shown in Figure 4.6. When we calculated peak value of these waveforms 27 V is found. Since DC-link was 30, volt modulation index again can be calculated close to 1. Because of inherent structure of the SPWM technique there is no way to obtain exact 1 modulation index in linear region ($0 < m < 1$). If the modulation index exceeds 1, this linear mode cannot be kept anymore and the special control strategy for over modulation is required.

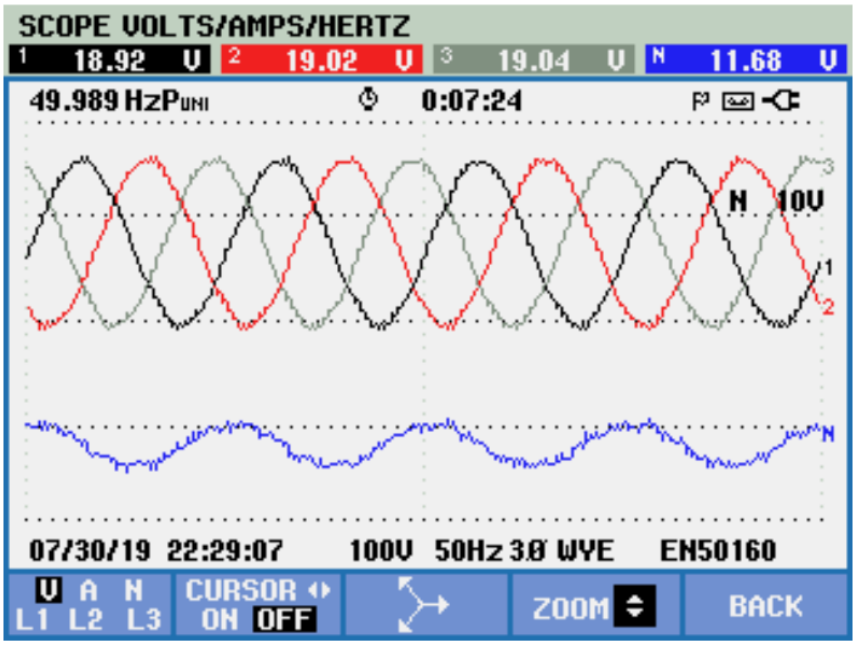

Figure 0.6. Fluke 435-II screen shot of the ouput voltage @ 30 V DC-link

Phase sequence was checked using Fluke 435-II and related measurement result is given in Figure 4.7. As shown from Figure 4.7. each phase separated from each other with 120° equally and fundamental voltages are balanced. It is clearly seen that inverter output voltage has 50 Hz operating frequency.

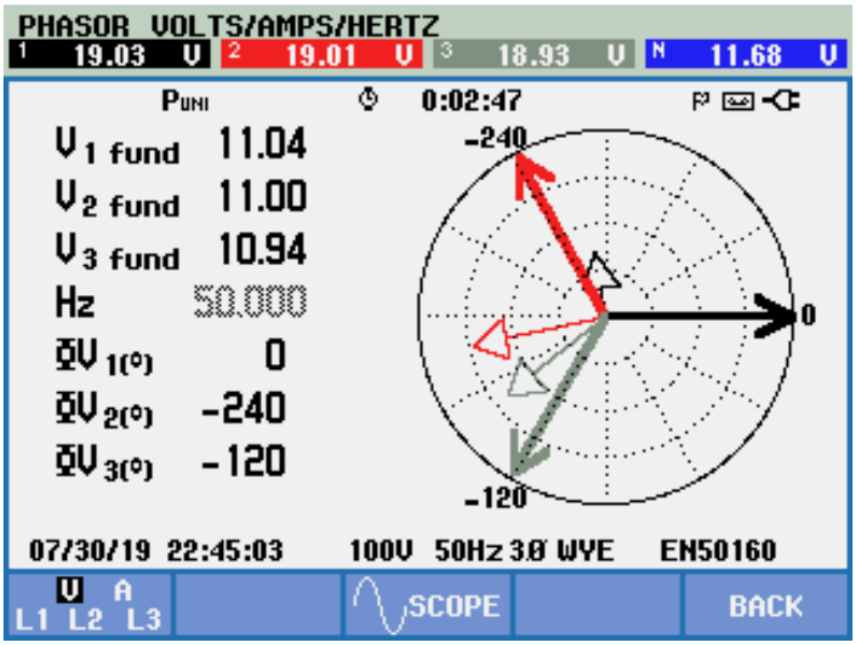

Figure 0.7. Phasor form of output phase voltages @30V DC-link level

Inverter was switched at 30 kHz and switching pattern is given in Figure 4.8.

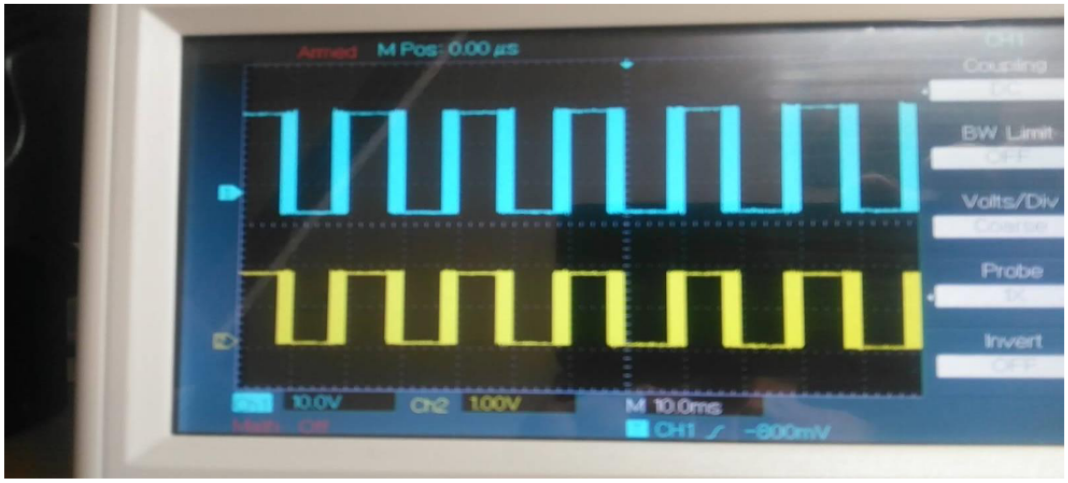

Figure 0.8. Inverter switching patterns

In order to check the thermal condition of the circuit the Flir one pro has been used. Thermal camera shows the areas with the higher temperatures in orange in figure 4.9.

Figure 4.9. Photo for the circuit by using the Flir one pro thermal camera.

In figure 4.10 the whole inverter's circuit is illustrated along with the power supply and TMS320F28 micro controller. The output voltage is presented in the oscilloscope.

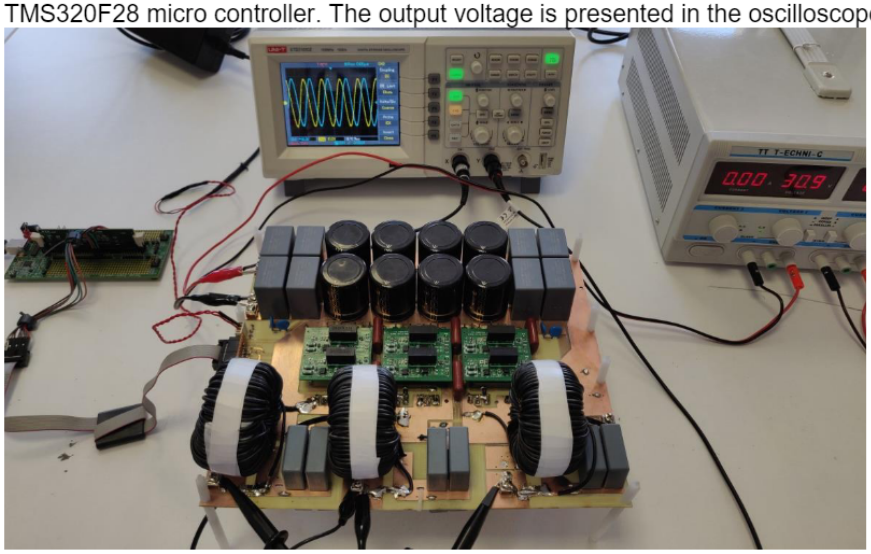

Figure 4.10. Inverter, Scope and Power Supply

Finally, to avoid any short circuit between upper and lower MOSFETs properly chosen dead band time was applied between switching patterns. 800 ns dead band is shown in Figure 4.8.

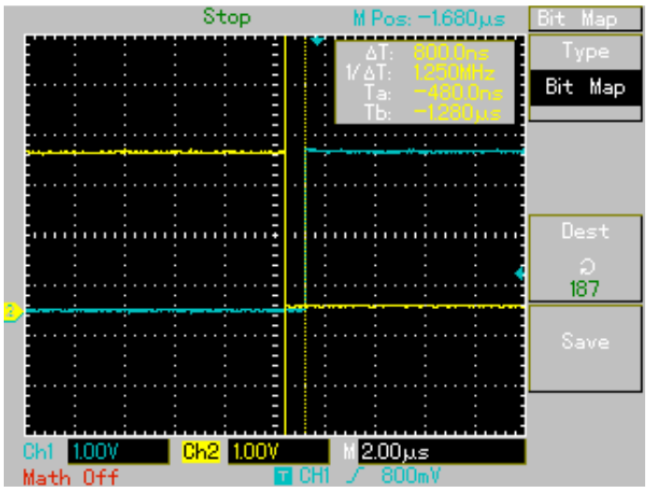

Figure 0.9. Dead band measurement

4.2. Recommendations

- By using the above design the power capability can be increased if two switches used in parallel.
- Paralleling inverter is also possible in this design to increase total amount of power with circulating current suppression mechanism.
- It is proposed to add the closed loop control mechanism to integrate the inverter with the renewable energy systems.
- Different load types can be studied along with analysing the performance under different power factors.
- Under heavy load condition frequency oscillations can be measured.
- For the measurement point, isolated sensors can be used to make noise free measurement.
- Grid connected test can be done with grid frequency synchronization.

TÜBİTAK
PROJE ÖZET BİLGİ FORMU

Proje Yürütücüsü:	Dr. Öğr. Üyesi BILAL EID
Proje No:	119E149
Proje Başlığı:	Sic Tabanlı Üç Fazlı İnvertör; Yüksek Verimli,Yüksek Güç Kapasitesine Sahip , Yenilenebilir Enerji Kaynakları Uygulamarı Için.
Proje Türü:	1002 - Hızlı Destek
Proje Süresi:	9
Araştırmacılar:	
Danışmanlar:	
Projenin Yürütüldüğü Kuruluş ve Adresi:	HASAN KALYONCU Ü.
Projenin Başlangıç ve Bitiş Tarihleri:	15/10/2019 - 15/07/2020
Onaylanan Bütçe:	41078.0
Harcanan Bütçe:	0.0
Öz:	In this Project 3 Phase 4-Wire 2-Level neutral point clamped SiC MOSFET based Voltage Source Inverter (VSI) was carried out. VSI was operated at 30 kHz switching frequency using neutral air cooling Aluminium (Al) heat sink. While designed VSI makes 3 phase connection possible, mid-point of the capacitors allows fourth wire connection as a neutral point. Properly designed, the LCL supply filter is used instead of L and LC type filters in this work since it provides a much better suppression at the modulation frequency. As a switching method Sinusoidal Pulse Width Modulation (SPWM) method was preferred and open loop control strategy was applied. Thanks to the SiC based switching device, high switching frequency operation was realized with very low losses and also filter size was reduced dramatically because of high switching frequency. Grid connection and renewable energy source compatibility took into consideration when electrical parameters were chosen. Proper gate driver design was also cared and suitable gate driver was designed. High power density was obtained at low volume and mass. Approximately 2.35 kW power was produced in unit volume (decimetre cube) and more than %98.5 efficiency was obtained.
Anahtar Kelimeler:	three phase inverter, Sillicon carbide Mosfet, wide-bandgap devices, renewable energy
Fikri Ürün Bildirim Formu Sunuldu Mu?:	Evet